IN THE CLAIMS

Cancel claims 3, 6, 16 and 19. Amend claims 1, 2, 4, 7, 8, 15, 17, 20, and 21.

Claim 1. (Currently Amended)
A modular Digital Locked Loop (DLL) architecture for generating a plurality of multiple phase clock signals comprising:

a single core frequency lock circuit comprising a delay element, a phase compare circuit, and a delay control circuit, for locking the single core frequency lock circuit to an external reference clock wherein the single core frequency lock circuit generates a plurality of internal clocks from, and in phase with, the external reference clock ;

a plurality of secondary phase lock circuits, each receiving an output from the single core frequency lock circuit, for ~~synchronizing~~ generating a plurality of internal clock signals to one of a plurality of selected phases of the external reference clock wherein each of the plurality of secondary phase lock circuits has inputs of the plurality of internal clocks and the external reference clock signal, and each secondary phase lock circuit produces a clock select digital code for selecting a particular one of the generated plurality of internal clocks.

Claim 2. (Currently Amended) The DLL architecture of claim 1, wherein the architecture is used for synchronization of an embedded DRAM system on a chip with on chip timing.

Claim 3. (Cancelled)

Claim 4. (Currently Amended) The DLL architecture of claim ~~3~~ 1, wherein the single core frequency lock circuit generates the plurality of internal clocks having the same

frequency as the external reference clock and which are phase displaced relative to each other.

Claim 5. (ORIGINAL) The DLL architecture of claim 4, wherein the plurality of internal clocks have a phase shift incrementally spaced by 360°/n where n is the number of the plurality of internal clocks.

Claim 6. (Cancelled)

Claim 7. (Currently Amended) The DLL architecture of claim ~~6~~ 1, wherein the clock select digital code is as input to a steering logic circuit signal for providing the selected particular one of the generated plurality of internal clocks.

Claim 8. (Currently Amended) The DLL architecture of claim ~~3~~ 1, wherein each secondary phase lock circuit includes a phase lock which selects a particular one of the generated plurality of internal clocks and passes it as a first input to a first port of a latch, the latch also receives the external reference clock as a second input at a clock port of the latch, and uses the first and second inputs to produce an input to control the phase lock.

Claim 9. (ORIGINAL) The DLL architecture of claim 8, wherein each secondary phase lock circuit counts in incremental steps, and at each step, a rising edge of the external reference clock at the clock port of the latch causes the latch to sample the first port, and this operation continues until a rising edge of the clock at the first port of the latch passes the rising edge of the external reference clock, and the count then hovers about a count at which the two rising edges are closely coincident.

Claim 10. (ORIGINAL)The DLL architecture of claim 9, wherein when the rising edge of the clock at the first port of the latch passes the rising edge of the external reference clock, the count is incrementally reduced, and the count then hovers about the count at which the two rising edges are closely coincident.

Claim 11. (ORIGINAL) The DLL architecture of claim 9, wherein the count controls a multiplexer to select and pass one of the plurality of generated internal clocks as an output of the secondary phase lock circuit.

Claim 12. (ORIGINAL) The DLL architecture of claim 9, wherein, in at least one secondary phase lock loop, the count is passed as a digital output to an adder which adds to the count a digital value representative of a phase increment or offset of the external reference clock.

Claim 13. (ORIGINAL) The DLL architecture of claim 9, wherein at least one secondary phase lock loop includes a mimic circuit which inserts a fixed time delay, introduced by the mimic circuit, into the phase lock loop.

Claim 14 (Currently Amended) A method of generating a plurality of multiple phase clock signals in a modular Digital Locked Loop (DLL) architecture, comprising:

locking a single core frequency lock circuit, comprising a delay element, a phase compare circuit and a delay control circuit, to an external reference clock which generates a plurality of internal clocks from, and in phase with the external reference clock by the single core frequency lock circuit;

~~synchronizing~~ generating a plurality of internal clock signals to one of a plurality of selected phases of the external reference clock by a plurality of secondary phase lock circuits, each receiving an output from the single core frequency lock circuit which produces a clock select digital code for selecting a particular one of the generated

plurality of internal clocks by each of the plurality of secondary phase lock circuits, each having inputs of the plurality of internal clocks and the external reference clock signal.

Claim 15. (Currently Amended) The method of claim 14, wherein the plurality of multiple phase clock signals are used for ~~including~~ synchronizing an embedded DRAM system on a chip with on chip timing.

Claim 16. (Cancelled)

Claim 17. (Currently Amended) The method of claim ~~16~~ 14, including generating the plurality of internal clocks having the same frequency as the external reference clock and which are phase displaced relative to each other by the single core frequency lock circuit.

Claim 18. (ORIGINAL) The method of claim 17, including generating the plurality of internal clocks with a phase shift incrementally spaced by 360°/n where n is the number of the plurality of internal clocks.

Claim 19. (Cancelled)

Claim 20. (Currently Amended) The method of claim ~~19~~ 14, including each of the secondary phase lock circuits inputting the clock select digital code to a steering logic circuit signal for providing the selected particular one of the generated plurality of internal clocks.

Claim 21. (Currently Amended) The method of claim ~~16~~ 14, including each of the secondary phase lock circuits selecting a particular one of the generated plurality of internal clocks and passing it as a first input to a first port of a latch by a phase lock, the

latch also receiving the external reference clock as a second input at a clock port of the latch, and using the first and second inputs to produce an input to control the phase lock.

Claim 22. (ORIGINAL) The method of claim 21, including each of the secondary phase lock circuits counting in incremental steps, and at each step, a rising edge of the external reference clock at the clock port of the latch causing the latch to sample the first port, and continuing this operation until a rising edge of the clock at the first port of the latch passes a rising edge of the external reference clock, and then hovering the count about a count at which the two rising edges are closely coincident.

Claim 23. (ORIGINAL) The method of claim 22, wherein when the rising edge of the clock at the first port of the latch passes the rising edge of the external reference clock, incrementally reducing the count, and hovering the count about a count at which the two rising edges are closely coincident.

Claim 24. (ORIGINAL) The method of claim 22, including the controlling a multiplexer with the count to select and pass one of the plurality of generated internal clocks as an output of the secondary phase lock circuit.

Claim 25. (ORIGINAL) The method of claim 22, further comprising, in at least one secondary phase lock loop, passing the count as a digital output to an adder which adds to the count a digital value representative of a phase increment or offset of the external reference clock.

Claim 26. (ORIGINAL) The method of claim 22, further comprising, in at least one secondary phase lock loop, including a mimic circuit which inserts a fixed time delay, introduced by the mimic circuit, into the phase lock loop.